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09/852,824	05/10/2001	Charles W.C. Lin	P002-2	5435

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EXAMINER	
GRAYBILL, DAVID E	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 09/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/852,824	LIN, CHARLES W.C.	
	Examiner	Art Unit	
	David E Graybill	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 February 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-119* is/are pending in the application.

4a) Of the above claim(s) *17,21,31-34,39,41-44,50-54,62-65,80-84 and 105-109* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15,16,18-20,22-30,35-38,45-49,55-61,66-79,85-104 and 110-119* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/465,024.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

The terminal disclaimer filed on 4-8-2 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of U.S. Patent No. 6,319,711 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Applicant's election with traverse of the species including depositing the solder on the metallization using electroplating, allegedly drawn to claims 15-30, 35-61 and 66-119; attaching the substrate using an adhesive, drawn to claims 15-38 and 40-119; applying heat to reflow the solder using a convection oven, drawn to claims 15-40 and 45-119; and the solder joint fills a bottom portion of the via hole without filling a tip portion, drawn to claims 15-119, in the reply filed on 2-21-3 is acknowledged. The traversal is on the ground(s) that the requirement "ignores the mandatory elements set forth in the M.P.E.P.." This is not found persuasive because the reasons for insisting on restriction as stated in MPEP 808.01(a) have been clearly met.

The requirement is still deemed proper and is therefore made FINAL.

Also, applicant's indication that the species including depositing the solder on the metallization using electroplating is drawn to claims 15-30, 35-61 and 66-119 is incorrect. The correct grouping of claims to which this species is drawn is claims 15, 16, 18-20, 22-30, 35-49, 55-61, 66-79, 85-104 and 110-119.

Applicant's argument that the species including substantially all of the solder joint is within the via hole and the solder joint fills a bottom portion of the via hole without filling a top portion are not patentably distinct is deemed persuasive and the requirement to elect one of these "species" is withdrawn.

Claims 17, 21, 31-34, 39, 41-44, 50-54, 62-65, 80-84 and 105-109 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected species, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 2-21-3.

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 20, 24, 25-30, 35-38, 45-49, 55-61, 66-79, 85-94, 96-104 and 110-119 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The undescribed subject matter is the claims 57, 58, 67 and 69 limitation, "essentially."

The undescribed subject matter is also the following negative limitations:

Claim 20, "without filling a top portion of the via hole after the reflowing";

Claim 24, "are the only materials in the via hole after the reflowing";

Claims 25 and 55, "prevents the via hole from exposing the pad";

Claim 46, "without filling a top portion of the via hole";

Claim 59, "are the only materials in the via hole after applying the heat";

Claim 60, "does not contact the solder on the bond site," "does not contact the pad," "does not contact the chip," and, "does not contact the solder joint and does not contact the chip";

Claim 68, "are the only materials in the via hole after applying the heat to reflow the solder";

Claims 70, 71, 75, 76, 85, 86, 90 and 91, "does not electrically connect the substrate and the chip";

Claims 72, 77, 87 and 92, "a bumpless pad";

Claims 73, 78, 88 and 93, "a solder-free pad";

Claims 74, 79, 89 and 94, "a bumpless solder-free pad";

Claim 96, "is the only material in the via hole that contacts the metallization after the reflowing";

Claim 97, "is the only material in the via hole that contacts the pad after the reflowing";

Claim 98, "is the only material that contacts the metallization and the pad after the reflowing";

Claim 99, "is the only conductor external to the chip that contacts the pad after the reflowing";

Claim 101, "is the only material in the via hole that contacts the metallization";

Claim 102, "is the only material in the via hole that contacts the pad";

Claim 103, "is the only material that contacts the metallization and the pad";

Claim 104, "is the only conductor external to the chip that contacts the pad";

Claim 111, "is the only material in the via hole that contacts the metallization";

Claim 112, "is the only material in the via hole that contacts the pad";

Claim 113, "is the only material that contacts the metallization and the pad";

Claim 114, "is the only conductor external to the chip that contacts the pad";

Claim 116, "is the only material in the via hole that contacts the metallization";

Claim 117, "is the only material in the via hole that contacts the pad";

Claim 118, "is the only material that contacts the metallization and the pad";

Claim 119, "is the only conductor external to the chip that contacts the pad."

To further clarify, any negative limitation or exclusionary proviso must have basis in the original disclosure. See Ex parte Grasselli, 231 USPQ 393 (Bd. App. 1983) aff'd mem., 738 F.2d 453 (Fed. Cir. 1984). The mere absence of a positive recitation is not basis for an exclusion.

Claims 15, 16, 18-20, 22-30, 35-38, 45-49, 55, 56, 59-61, 66, 68, 70-79, 85-104 and 110-119 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. Specifically, claims 57, 58, 67 and 69, recite essential limitations preceded by the term "essentially," however, claims 15, 16, 18-20, 22-30, 35-38, 45-49, 55, 56, 59-61, 66, 68, 70-79, 85-104 and 110-119 fail to recite these essential limitations. A claim that omits an element which applicant describes as an essential or critical feature of the invention originally disclosed does not comply with the written

description requirement. See Gentry Gallery, 134 F.3d at 1480, 45 USPQ2d at 1503; In re Sus, 306 F.2d 494, 504, 134 USPQ 301, 309 (CCPA 1962) . A claim which omits matter disclosed to be essential to the invention as described in the specification or in other statements of record may also be subject to rejection under 35 U.S.C. 112, para. 1, as not enabling, or under 35 U.S.C. 112, para. 2. See In re Mayhew, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976); In re Venezia, 530 F.2d 956, 189 USPQ 149 (CCPA 1976); and In re Collier, 397 F.2d 1003, 158 USPQ 266 (CCPA 1968). See also MPEP § 2163IB and § 2172.01.

In the rejections infra, generally, reference labels are recited only for the first recitation of identical claim elements.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High

Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 15, 16, 18-20, 22-27, 29, 30, 36-38, 45-49, 70-79 and 95-104 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Hino.

At column 4, line 19 to column 5, line 56; column 7, lines 10-16; column 7, line 65 to column 8, line 22; and column 9, lines 1-30, Hino discloses the following:

A method of making a flip chip assembly, comprising: attaching a substrate 2 to a semiconductor chip 3, wherein the substrate includes a dielectric layer 6 and metallization 13, the dielectric layer includes first 6b and second 6a surfaces that are opposite one another and a via hole 64 that extends between the first and second surfaces, the metallization is disposed on walls of the via hole, the chip includes a terminal pad 12 that is aligned with the via hole, and a reflowable material 15 that contains solder contacts the metallization and the pad; and then reflowing the reflowable material to provide an electrical connection between the metallization and the pad; wherein the reflowable material is deposited on the metallization before attaching the substrate to the chip, and during the reflowing the reflowable

material wets and flows on an exposed portion of the pad beneath the via hole; wherein the pad is directly beneath substantially all surface area defined by the via hole after the attaching; wherein the metallization is electrolessly plated on the walls of the via hole; wherein the reflowable material fills a bottom portion of the via hole without filling a top portion of the via hole after the reflowing; wherein the substrate remains at a fixed position relative to the chip during the reflowing; wherein substantially all of the reflowable material is within the via hole after the reflowing "the conductive paths 7 and 8 are formed only to reach the same surface level with both surfaces 6a and 6b"; wherein the metallization and the reflowable material are the only materials in the via hole after the reflowing; attaching the substrate to the chip using an adhesive that does not electrically connect the substrate and the chip; attaching the substrate to the chip using an adhesive that is sandwiched between and contacts the substrate and the chip and does not electrically connect the substrate and the chip; wherein the pad is a bumpless pad; wherein the pad is a solder-free pad; wherein the pad is a bumpless solder-free pad; wherein the reflowable material extends continuously between the first and second surfaces in the via hole after the reflowing; wherein the reflowable material is the only material in the via hole that contacts the metallization after the reflowing; wherein the reflowable material is the only material in the via hole that contacts the pad

after the reflowing; wherein the reflowable material is the only material that contacts the metallization and the pad after the reflowing; wherein the reflowable material is the only conductor external to the chip that contacts the pad after the reflowing.

A method of making a flip chip assembly, comprising the following steps in the sequence set forth: providing a substrate that includes a dielectric layer, wherein the dielectric layer includes first and second surfaces that are opposite one another and a via hole that extends between the first and second surfaces; depositing metallization on walls of the via hole; depositing solder on the metallization such that the solder is disposed in the via hole; attaching the substrate to a semiconductor chip that includes a terminal pad, wherein the first surface faces away from the chip, the second surface faces towards the chip, the via hole is aligned with the pad and the solder contacts the pad; and applying heat to reflow the solder to form a solder joint that contacts and electrically connects the metallization and the pad and prevents the via hole from exposing the pad; depositing the metallization on the walls using electroless plating; depositing the metallization on the walls such that substantially all of the metallization is within the via hole; depositing the metallization on the walls such that the metallization is aligned with the second surface; depositing the solder on the metallization using electroplating; attaching the substrate to the chip such

that the via hole exposes the pad (to 7); attaching the substrate to the chip such that the pad is directly beneath substantially all surface area defined by the via hole; attaching the substrate to the chip using an adhesive 20 between the substrate and the chip; applying the heat to reflow the solder such that substantially all of the solder joint is within the via hole; applying the heat to reflow the solder such that the solder joint fills a bottom portion of the via hole without filling a top portion of the via hole; applying the heat to reflow the solder such that the solder wets and covers an exposed portion of the pad; applying the heat to reflow the solder while maintaining the substrate at a fixed position relative to the chip; wherein the metallization and the solder joint are the only materials in the via hole after applying the heat; attaching the substrate to the chip using an adhesive that does not electrically connect the substrate and the chip; attaching the substrate to the chip using an adhesive that is sandwiched between and contacts the substrate and the chip and does not electrically connect the substrate and the chip; wherein the pad is a bumpless pad; wherein the pad is a solder-free pad; wherein the pad is a bumpless solder-free pad; wherein the solder joint extends continuously between the first and second surfaces in the via hole; wherein the solder joint is the only material in the via hole that contacts the metallization; wherein the solder joint is the only material in the via hole that contacts the pad; wherein the solder joint is the only material

that contacts the metallization and the pad; wherein the solder joint is the only conductor external to the chip that contacts the pad.

To further clarify the disclosure of the pad beneath the via hole, the pad is directly beneath the via, and the reflowable material fills a bottom portion of the via hole without filling a top portion, the disclosed process of Hino is not limited to an absolute frame of reference or otherwise limited to a particular orientation, and it is inherent that there is a frame of reference wherein the pad is beneath the via hole, the pad is directly beneath the via, and the reflowable material fills a bottom portion of the via hole without filling a top portion.

To further clarify the disclosure wherein the substrate remains at a fixed position relative to the chip during the reflowing, this process is an inherent property of the embodiment wherein "the conductive paths 7 and 8 are formed only to reach the same surface level with both surfaces 6a and 6b." Also, in the embodiment of FIG. 9, the substrate remains at a fixed position in the horizontal direction relative to the chip during the reflowing.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 40 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hino as applied to claim 25, and further in combination with Gaynes (6165885).

Hino does not appear to explicitly disclose applying the heat to reflow the solder using a convection oven.

Nonetheless, at column 21, lines 15-17, Gaynes discloses applying heat to reflow solder using a convection oven. Moreover, it would have been obvious to combine this process of Gaynes with the process of Hino because it would facilitate the reflow of Hino.

The art made of record and not applied to the rejection is considered pertinent to applicant's disclosure. It is cited primarily to show inventions similar to the instant invention.

For information on the status of this application applicant should check PAIR: Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alternatively, applicant may contact the File Information Unit at (703) 308-2733. Telephone status inquiries should not be directed to the examiner. See MPEP 1730VIC, MPEP 203.08 and MPEP 102.

Any other telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (571) 272-1930. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.
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David E. Graybill
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Art Unit 2827

D.G.
17-Sep-04